

WALLES
Serial No. 09/902,804

Atty Dkt: 2380-380
Art Unit: 2664

REMARKS/ARGUMENTS

Reexamination of the captioned application is respectfully requested.

A. SUMMARY OF THIS AMENDMENT

By the current amendment, Applicants basically:

1. Editorially amend claims 3 and 12.
2. Respectfully traverse all prior art rejections.

B. PATENTABILITY OF THE CLAIMS

Claims 1-19 stand rejected under 35 USC §102(e) as being anticipated by U.S. Patent 6,700,893 to Radha et al. All prior art rejections are respectfully traversed for at least the following reasons.

Applicants persist with the traversal that Radha does not teach or suggest the claimed processing chain. Both independent claim 1 and independent claim 10 clearly require that the processing chain comprise

plural processing units through which a packet of the media stream is routed, each of the plural processing units generating an intra-node performance monitoring packet which includes an indication of time spent by the packet of the media stream in the respective processing unit

The fifth enumerated paragraph of the Final Office Action appears to allege that the IDT buffers, delay budget controller, and re-transmission controller are processing units (by virtue of being implemented in a personal computer (PC) or the like). Yet in such case these Radha elements (IDT buffers, delay budget controller, and re-transmission controller) are implemented by the same processor, and therefore are not plural processing units of a chain.

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[In view of enumerated paragraph 5 of the Office Action, Applicant no longer believes the Examiner to be asserting that Radha's "access units" are the alleged processors. As previously explained, Radha's "access units" are instead merely a grouping of packets in IDT buffer 132 (see the last full ¶ of col. 7 and the ¶ bridging col. 7 and col. 8 of Radha).]

Moreover, of the three elements identified in enumerated paragraph 5 of the Final Office Action, the Radha packets themselves only travel through IDT buffer 132. The Radha packets do not travel through plural separate processing units. Thus, the Radha packets do not travel through processing units of a chain.

Nor do any units through which the Radha packets may travel generate any further distinct packets which serve for intra-node performance monitoring. Admittedly Radha has a buffer manager for monitoring delay in the one buffer. But the buffer itself is not a processor, nor does it generate separate packets for communicating "time spent" information to a performance monitoring unit. In fact, no unit of Radha appears to generate any such packets.

Applicants beg that the convoluted disclosure of Radha not be misapprehended. The Examiner is referred to the first two paragraphs of column 16 of Radha, which appear to give clearer summary of the Radha teaching. Moreover, from this and other portions of Radha, it will be appreciated that the delay of concern to Radha is not delay in the node itself, but overall network delay.

Therefore, not teaching or suggesting a chain of processing units, not having any processing unit which generates an intra-node performance monitoring packet, and not being concerned with intra-node delay, Radha lacks many significant aspects of Applicant's claim and provides no sustainable basis for denial of patentability.

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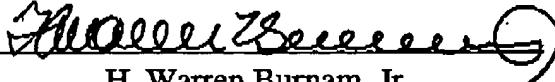
C. MISCELLANEOUS

In view of the foregoing and other considerations, all claims are deemed in condition for allowance. A formal indication of allowability is earnestly solicited.

The Commissioner is authorized to charge the undersigned's deposit account #14-1140 in whatever amount is necessary for entry of these papers and the continued pendency of the captioned application.

Should the Examiner feel that an interview with the undersigned would facilitate allowance of this application, the Examiner is encouraged to contact the undersigned.

Respectfully submitted,
NIXON & VANDERHYE P.C.

By: 
H. Warren Burnam, Jr.
Reg. No. 29,366

HWB:lsh
1100 North Glebe Road, 8th Floor
Arlington, VA 22201-4714
Telephone: (703) 816-4000
Facsimile: (703) 816-4100